

FIG. 1 is a block diagram of a computer system 100. The system 100 includes a processor 110, a memory controller hub (MCH) 130, an input/output controller hub (ICH) 150, and a mass storage device 170. The processor 110 includes a processor core 112 and a cache unit 115. The MCH 130 includes a chipset cache 135. The ICH 150 is connected to various I/O devices 180₁ through 180_K, a CD ROM 172, a floppy 174, and a hard drive 176. The MCH 130 is connected to system memory 140. The ICH 150 is connected to the mass storage device 170. The processor 110, MCH 130, and ICH 150 are connected to a host bus 120. The mass storage device 170 is connected to the ICH 150. The I/O devices 180₁ through 180_K are connected to the ICH 150. The CD ROM 172, floppy 174, and hard drive 176 are connected to the mass storage device 170. The system memory 140 is connected to the MCH 130. The host bus 120 is connected to the processor 110, MCH 130, and ICH 150.

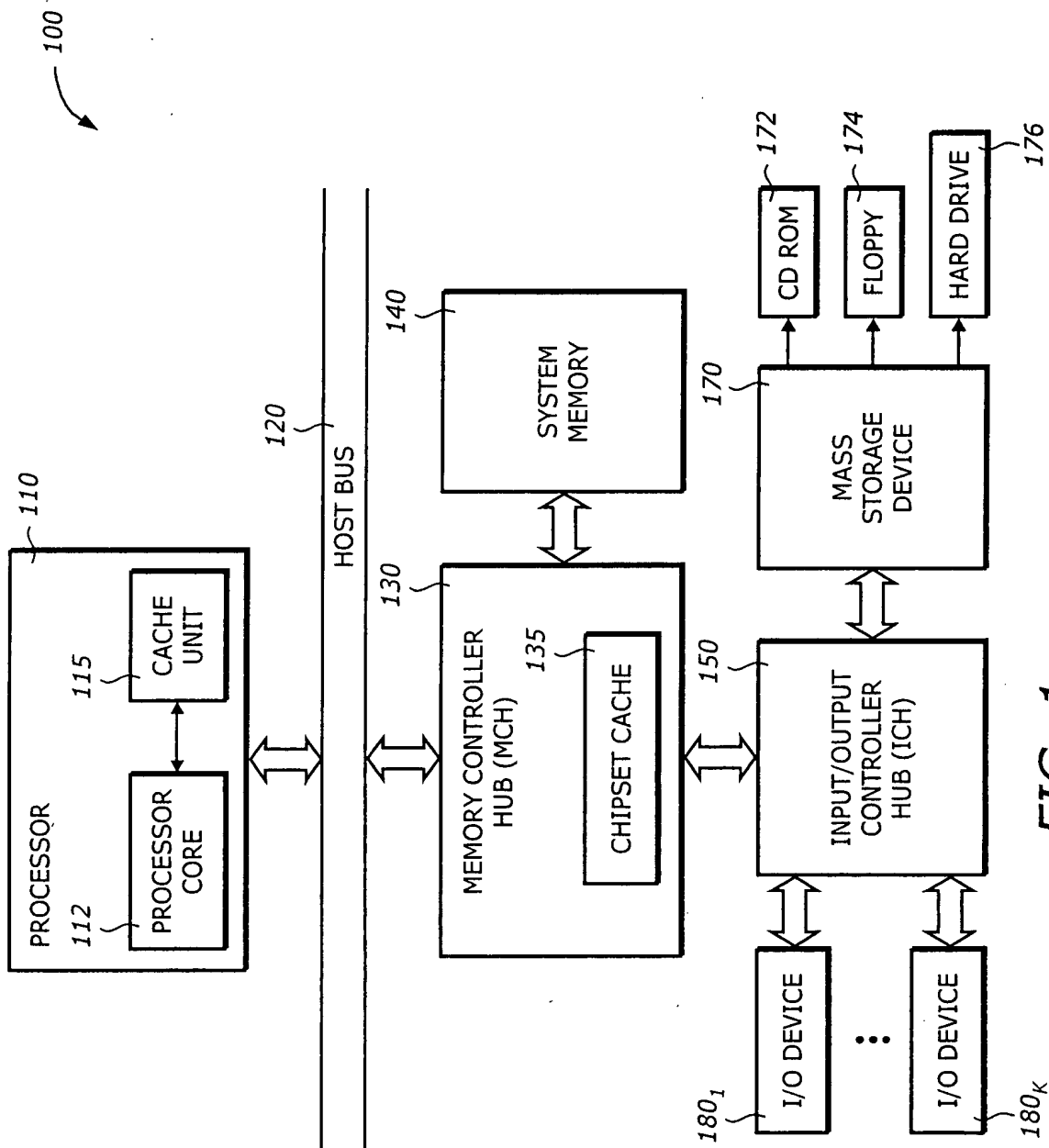


FIG. 1

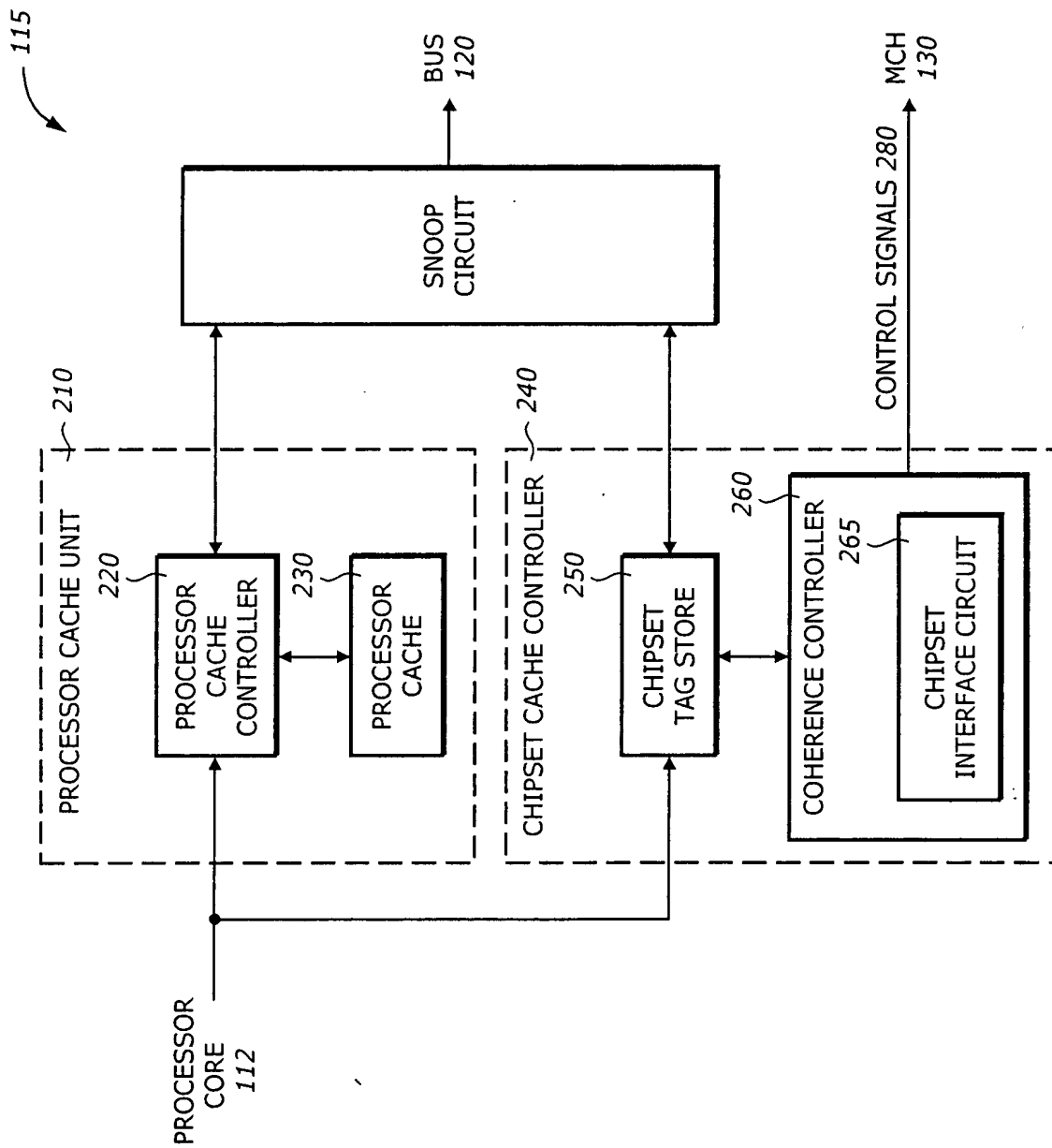


FIG. 2

Figure 3 shows the operation of the cache access type = read. The cache access type = read is performed by the processor. The cache access type = read is performed by the processor.

CACHE ACCESS TYPE = READ				
CACHE VALID INDICATOR	FLUSH INDICATOR	SET IDENTIFIER	OPERATION PERFORMED BY CHIPSET	
NEGATED	NEGATED	SSSS	READ DATA FROM MEMORY INTO CACHE SET SSSS IN CHIPSET. DATA IS SUBSEQUENTLY RETURNED TO PROCESSOR	
NEGATED	ASSERTED	SSSS	READ DATA FROM MEMORY INTO CACHE SET SSSS IN CHIPSET. FLUSH EXISTING DATA IN CACHE SET SSSS TO MEMORY. DATA IS SUBSEQUENTLY RETURNED TO PROCESSOR	
ASSERTED	NEGATED	SSSS	READ DATA FROM CACHE SET SSSS IN CHIPSET AND RETURN DATA TO PROCESOR	
ASSERTED	ASSERTED	SSSS	NOT VALID	

FIG. 3

CACHE ACCESS TYPE = WRITE

CACHE VALID INDICATOR	FLUSH INDICATOR	SET IDENTIFIER	OPERATION PERFORMED BY CHIPSET
NEGATED	NEGATED	SSSS	WRITE DATA FROM PROCESSOR TO CACHE SET SSSS IN CHIPSET AND IMMEDIATELY TO MEMORY. PUT LINE INTO CLEAN STATE
NEGATED	ASSERTED	SSSS	WRITE DATA FROM PROCESSOR TO CACHE SET SSSS IN CHIPSET. FLUSH EXISTING DATA AT CHIPSET TO MEMORY. WRITE DATA IMMEDIATELY TO MEMORY
ASSERTED	NEGATED	SSSS	WRITE DATA FROM PROCESSOR TO CACHE SET SSSS IN CHIPSET
ASSERTED	ASSERTED	SSSS	WRITE DATA FROM PROCESSOR TO CACHE SET SSSS IN CHIPSET. FLUSH EXISTING DATA TO MEMORY

FIG. 4